

74LVX00

Low Voltage Quad 2-Input NAND Gate

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

General Description

The LVX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

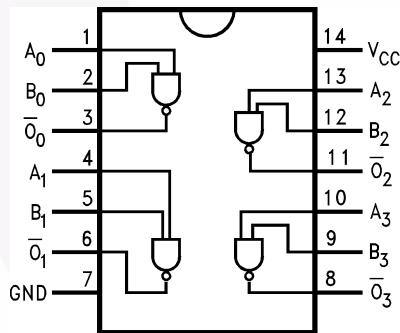
Ordering Information

Order Number	Package Number	Package Description
74LVX00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

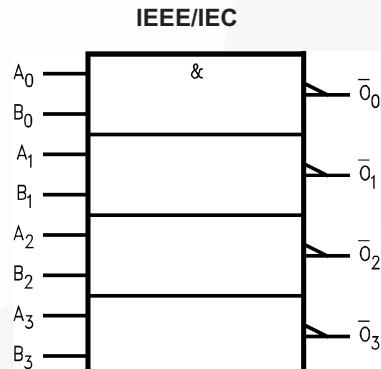
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
A _n , B _n	Inputs
O _n	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current, $V_I = -0.5V$	-20mA
V_I	DC Input Voltage	-0.5V to 7V
I_{OK}	DC Output Diode Current $V_O = -0.5V$	-20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 25mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
P	Power Dissipation	180mW

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 3.6V
V_I	Input Voltage	0V to 5.5V
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

Note:

- Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A = +25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V _{IL}	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V _{OH}	HIGH Level Output Voltage	2.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -50µA	1.9	2.0		1.9		V
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -50µA	2.9	3.0		2.9		
			V _{IN} = V _{IL} or V _{IH} , I _{OH} = -4mA	2.58			2.48		
V _{OL}	LOW Level Output Voltage	2.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 50µA		0.0	0.1		0.1	V
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 50µA		0.0	0.1		0.1	
			V _{IN} = V _{IL} or V _{IH} , I _{OL} = 4mA			0.36		0.44	
I _{IN}	Input Leakage Current	3.6	V _{IN} = 5.5V or GND			±0.1		±1.0	µA
I _{CC}	Quiescent Supply Current	3.6	V _{IN} = V _{CC} or GND			2.0		20.0	µA

Noise Characteristics⁽²⁾

Symbol	Parameter	V _{CC} (V)	C _L (pF)	T _A = 25°C		Units
				Typ.	Limit	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	50	0.3	0.5	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	50	-0.3	-0.5	V
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

Note:

2. Input t_r = t_f = 3ns

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	C _L (pF)	T _A = +25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t _{PLH} , t _{PHL}	Propagation Delay Time	2.7	15		5.4	10.1	1.0	12.5	ns
			50		7.9	13.6	1.0	16.0	
		3.3 ± 0.3	15		4.1	6.2	1.0	7.5	
			50		6.6	9.7	1.0	11.0	
t _{OSLH} , t _{OSSH}	Output to Output Skew ⁽³⁾	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

Note:

3. Parameter guaranteed by design t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSSH} = |t_{PHLm} - t_{PHLn}|

Capacitance

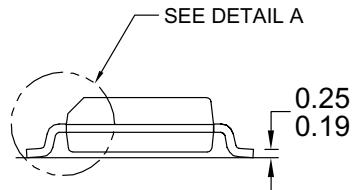
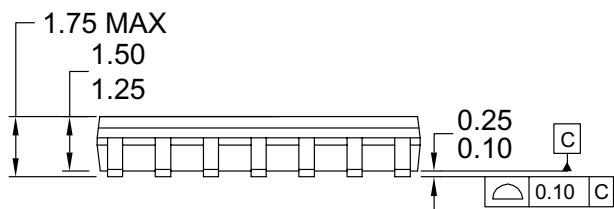
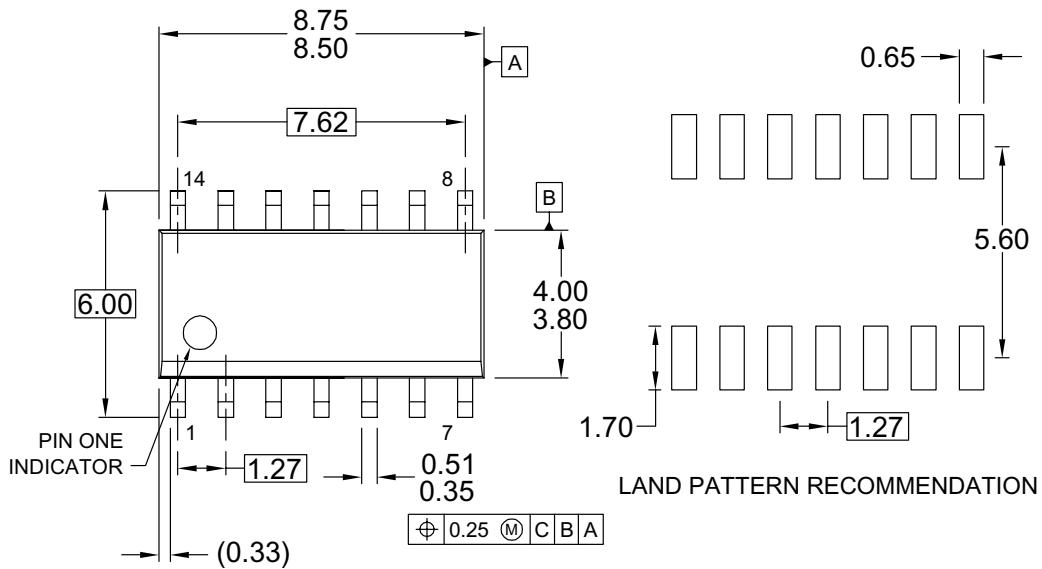
Symbol	Parameter	T _A = +25°C			T _A = -40°C to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance ⁽⁴⁾		19				pF

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr.})} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{4 \text{ (per Gate)}}$$

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

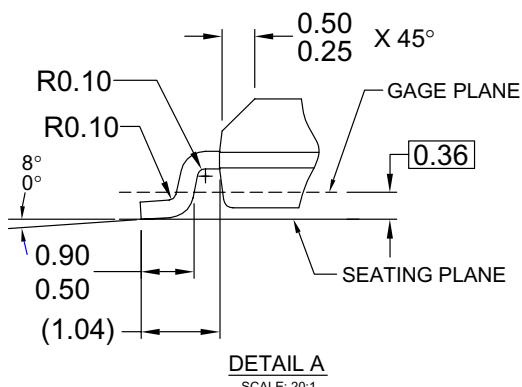


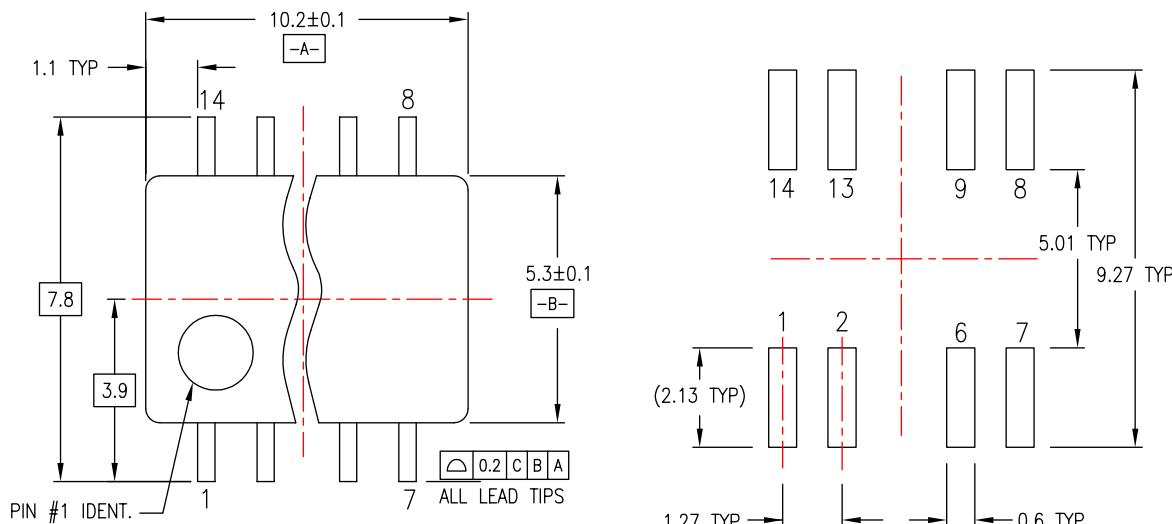
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

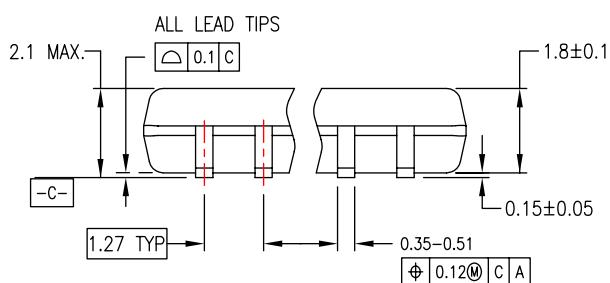
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Physical Dimensions (Continued)



LAND PATTERN RECOMMENDATION

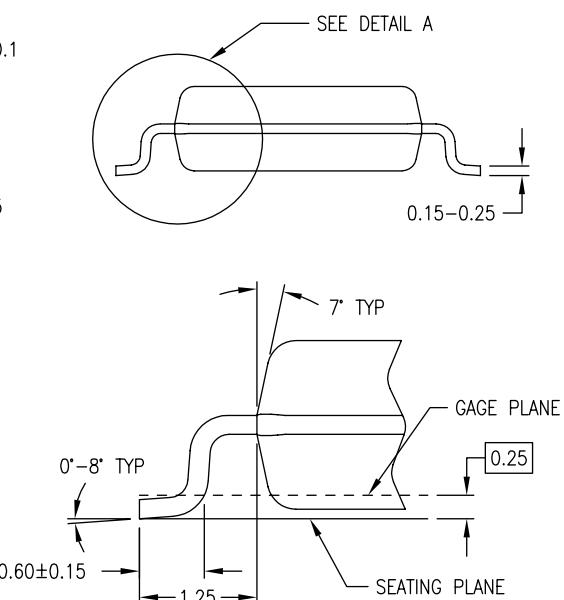


DIMENSIONS ARE IN MILLIMETERS

NOTES:

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DRFVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

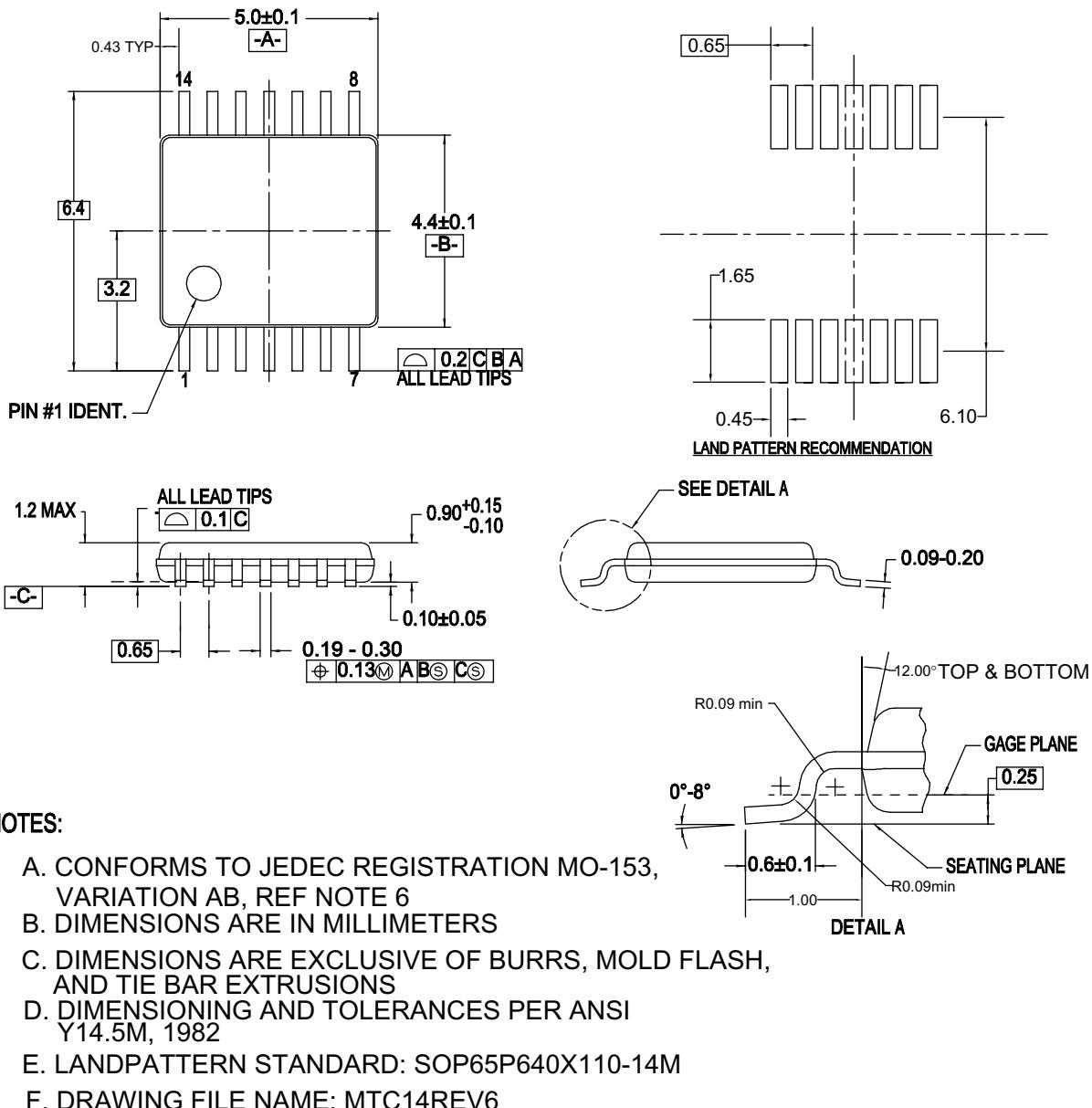


Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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